Abstract of the Disclosure:

A method of generating a test pattern for simulating and/or testing the layout of an integrated circuit includes the steps of generating a set of test patterns on a random basis, applying the set of test patterns to the integrated circuit using an automatic test equipment, determining the outputs of the integrated circuit, processing the outputs to determine whether predetermined test criteria are met, and, depending on a result of the processing step, generating a new set of test patterns based on the old set of test patterns by using a genetic algorithm. Accordingly, the method employs a genetic algorithm to optimize a set of random patterns based on measurements by using an automatic test equipment. Thereby, a set of worst case noise patterns can be selected automatically.

MB/kf